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AUTOMATIC LATCH COMPRESSION/REDUCTION

Abstract

The disclosure presents a method of designing an integrated circuit having latches. The invention first prepares a logical design of logic devices and latches and then creates a physical design by positioning the logic devices and the latches within the integrated circuit based on the logical design. During the process of creating the physical design the invention eliminates redundant latches by combining latches which do not transition during the same clock cycle, latches which do not relate to the same logical function, latches which are in the same clock domain, and latches that are within a given physical proximity of each other. The invention determines whether latches transition during the same clock cycle by running a simulation of an initial physical design and recording the latches that transition during each clock cycle. The invention also determines whether an adequate timing slack exists between transitions of latches that do not transition during the same clock cycle. The foregoing process of eliminating redundant latches comprises replacing at least two latches with a single latch. The

process of eliminating redundant latches produces a revised physical design, and the invention tests the revised physical design to determine whether the revised physical design performs as expected.